

**UNITED STATES DEPARTMENT OF COMMERCE****Patent and Trademark Offic**

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|-------------|-----------------------------------|---------------------------------------|
| 09/129, 675 | 08/05/98 | HARARI | E HARI. 006USS |
| <input type="checkbox"/> 020227 | | MM91/0316 | <input type="checkbox"/> EXAMINER |
| MAJESTIC PARSONS SIEBERT & HSUE SUITE 1100 FOUR EMBARCADERO CENTER SAN FRANCISCO CA 94111-4106 | | | TRAN, A |
| | | <input type="checkbox"/> ART UNIT | <input type="checkbox"/> PAPER NUMBER |
| | | 2824 | |
| | | DATE MAILED: | 03/16/00 |

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

| | | |
|------------------------------|--------------------------------------|--------------------------------------|
| Office Action Summary | Application No. 09/129,675 | Applicant(s) HARARI et al. |
| | Examiner Andrew Q. Tran | Group Art Unit 2824 |

Responsive to communication(s) filed on Dec 3, 1998, AUGUST 10, 1999 & OCTOBER 29, 1999.
 This action is **FINAL**.

Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed 03/14/00 in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 1 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

Claim(s) 63-111 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

Claim(s) _____ is/are allowed.

Claim(s) _____ is/are rejected.

Claim(s) _____ is/are objected to.

Claims 63-111 are subject to restriction or election requirement.

Application Papers

See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

The drawing(s) filed on _____ is/are objected to by the Examiner.

The proposed drawing correction, filed on _____ is approved disapproved.

The specification is objected to by the Examiner.

The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

All Some* None of the CERTIFIED copies of the priority documents have been received.

received in Application No. (Series Code/Serial Number) _____.

received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

Notice of References Cited, PTO-892

Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

Interview Summary, PTO-413

Notice of Draftsperson's Patent Drawing Review, PTO-948

Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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The Preliminary Amendments filed respectively on December 03, 1998, August 10, 1999 and October 29, 1999 have all been received and placed of record.

Claims 1-62 been canceled.

Claims 92-111 been added.

Claims 63-111 pending. The indicated allowability of claims 63-91 is withdrawn.

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 63-91, drawn to a nonvolatile semiconductor memory device, classified in class 365, subclass 185.22.
- II. Claims 92-97, drawn to a nonvolatile semiconductor memory device with redundancy, classified in class 365, subclass 185.09.
- III. Claim 98, drawn to a nonvolatile semiconductor memory device with a cache memory, classified in class 365, subclass 189.05.
- IV. Claim 99, drawn to a nonvolatile semiconductor memory system, classified in class 365, subclass 230.06.

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V. Claims 100-111, drawn to a method for programming a nonvolatile semiconductor memory device, classified in class 365, subclass 185.33.

The inventions are distinct, each from the other because:

Inventions of Group II and Group I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the nonvolatile semiconductor memory device with redundancy of the invention of Group II could use other nonvolatile semiconductor memory device other than the one claimed in the Group I invention. The subcombination has separate utility such as a nonvolatile semiconductor memory device by itself, at least evidenced by U.S. Patent No. 5,657,270 to Ohuchi et al., mentioned in the Preliminary Amendment filed August 05, 1998, page 28, lines 8-10.

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Inventions of Group III and Group I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the nonvolatile semiconductor memory device with a cache memory as claimed in the Group III invention could use other nonvolatile semiconductor memory device, known in the art, other than the device claimed in the Group I invention. The subcombination has separate utility such as a nonvolatile semiconductor memory device by itself, as set forth above.

Inventions of Group I and Group IV are distinct because Group I invention recites a nonvolatile semiconductor memory device comprising a plurality of bit lines, a plurality of word lines, a memory cell array, and a plurality of programming circuits; while on the other hand, the Group IV invention distinctly claims a nonvolatile semiconductor memory system comprising a plurality of memory cells, a plurality of bit lines,

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a plurality of data storing circuits, a plurality of data detecting circuits, and a write end detecting circuit. Therefore the inventions of Group I and Group IV each requires a different circuit structure for its own nonvolatile semiconductor memory device, as claimed.

Inventions of Group I and Group V are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case, the method for programming a nonvolatile semiconductor memory device, as claimed in the Group V invention, can be practiced with another materially different product, such as another nonvolatile semiconductor memory device known in the art, other than the nonvolatile semiconductor memory device as claimed in the Group I invention.

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Inventions of Group II and Group III are distinct because one requires a redundancy scheme while the other requires a cache memory.

Inventions of Group II and Group IV are distinct for the reasons similar to setting forth above to show the distinction between the inventions of Group I and Group IV.

Inventions of Group II and Group V are distinct for the reasons similar to setting forth above to show the distinction between the inventions of Group I and Group V.

Inventions of Group III and Group IV are distinct for the reasons similar to setting forth above in proving the distinction between Group I and Group IV.

Inventions of Group III and Group V are distinct for the reasons similar to setting forth above in proving the distinction between Group I and Group V.

Inventions of Group IV and Group V are related as product and process of use. The inventions can be shown to be distinct

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if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case, the method for programming a nonvolatile semiconductor memory device, as claimed in the Group V invention, can be practiced with another materially different product, such as other known nonvolatile semiconductor memory system.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Papers related to this application may be submitted to Technology Center 2800, Group 2810 by facsimile transmission.

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Papers should be faxed to Group 2810 via the Fax Center. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (October 19, 1988). The Fax Center number is (703) 308-7722 or (703) 308-7724.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Q. Tran whose telephone number is (703) 305-3495.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956.



ANDREW Q. TRAN
PRIMARY EXAMINER

Andrew Q. Tran
March 14, 2000